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EXAMINER	
BUTLER, DENNIS	
ART UNIT	**PAPER NUMBER**
2115	5

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/707,585	VERDUN, GARY J.
	Examiner	Art Unit
	Dennis M. Butler	2115

PRO

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to the application filed on November 6, 2000. Claims 1-15 are pending.

2. Applicant is advised that should claim 3 be found allowable, claim 4 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 5-6 and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Pole, II, U. S. Patent 6,496,888.

Per claim 1:

A) Pole, II teaches the following claimed items:

1. a processor with various power state conditions that performs at a selectable operating mode with processor 202 of figure 2 and at column 2, line 61 – column 3, line 25;

2. a north bridge controller with chipset logic 214 of figure 2 and at column 4, lines 15-26;

3. a south bridge controller with bus bridge 226 of figure 2 and at column 4, lines 32-45;

4. a clock at column 4, lines 46-55 and at column 5, lines 40-49;

5. a power supply with the AC power supply corresponding to the AC power source and/or the battery at column 2, line 61 – column 3, line 10;

6. a logic device interfaces to the above elements that asserts a transition to a different operating mode on the processor while the processor is in a deep sleep state with the chip set logic and the bus ratio strap option logic of figures 2 and 3, with figure 4B, at column 3, lines 11-25, at column 5, line 11-39 and at column 6, line 41 – column 7, line 4;

7. the clock providing a frequency and the power supply providing a voltage matched to the different operating mode upon transition at column 2, line 61 – column 3, line 10.

Per claims 2, 5 and 6:

Pole describes the logic device monitoring a reset condition of the processor, waiting for the reset to be deasserted and asserting a performance mode

transition with figure 4B and at column 6, line 60 – column 7, line 4. Pole describes asserting either the high performance mode or the low performance mode during normal processor power up sequence (system power up) that includes accessing a ROM (loading system settings from ROM) at column 5, line 67 – column 6, line 10.

Per claim 13:

A) Pole, II teaches the following claimed items:

1. a processor with various power state conditions that performs at a selectable operating mode with processor 202 of figure 2 and at column 2, line 61 – column 3, line 25;

2. waiting for the processor to reach a reset state (deep sleep state/mode) with elements 450 and 460 of figure 4B and at column 6, lines 41-63;

3. resetting the processor with element 470 of figure 4B and at column 6, lines 60-63;

4. asserting a performance mode change on the processor with element 480 of figure 4B and at column 6, line 63 – column 7, line 4.

Per claims 14 and 15:

Pole describes asserting either the high performance mode or the low performance mode during normal processor power up sequence (system power up) that includes accessing a ROM (loading system settings from ROM) at column 5, line 67 – column 6, line 10. Since Pole describes selecting either a high or low performance mode during system boot, the system clearly can be set

to assert the high performance mode during normal processor power up sequence (system power up).

2. Claims 3-4 and 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pole, II, U. S. Patent 6,496,888 in view of Pole, II et al., U. S. Patent 6,272,642.

Per claims 3-4, 11 and 12:

A) Pole, II teaches the following claimed items:

1. a processor with various power state conditions that performs at a selectable operating mode with processor 202 of figure 2 and at column 2, line 61 – column 3, line 25;

2. transitioning the processor into a different operating mode with figures 2, 3 and 4B, at column 3, lines 11-25, at column 5, line 11-39 and at column 6, line 41 – column 7, line 4.

B) The claims seem to differ from Pole, II in that Pole, II fails to explicitly teach passing control signals from a north bridge or south bridge controller capable of placing the processor in a deep sleep state as claimed.

C) However, Pole, II describes that the chip set logic is divided into a North Bridge and a South Bridge and that the logic could be included in the North or South Bridge or in a single chip that integrates both bridges at column 4, line 64 – column 5, line 39. Pole, II further describes placing the bus ratio register that sets the operating mode of the processor into the chipset component that generates control signals during a processor reset sequence at column 5, lines 11-17. Pole, II describes placing the processor in a deep sleep state and

transitioning it to a different operating mode with figure 4b. Pole, II suggests that the chip set/bridge passes control signals capable of placing the processor in a deep sleep state using system control logic and system management bus interface of the chip set at column 5, lines 19-21, at column 7, lines 50-55 and at column 8, lines 24-46. However, Pole, II does not explicitly recite that control signals capable of placing the processor in a deep sleep state are passed from the chip set or bridge. Pole, II et al teach that it is known to include a bridge that passes control signals capable of placing the processor in a deep sleep state with figures 1, 2 and 4, at column 3, line 66 – column 4, line 30 and at column 4, lines 55-61. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a north or a south bridge that passes control signals capable of placing the processor in a deep sleep state, as suggested by Pole, II in view of Pole, II et al, in order to incorporate the bus ratio register into a chip set that generates control signals during the deep sleep and reset sequence for transitioning the processor into a different operating mode. One of ordinary skill in the art would have been motivated to combine Pole, II and Pole, II et al because of Pole, II suggestion of incorporating the bus ratio register into a chip set (north and/or south bridge) that generates control signals during the reset sequence at column 5, lines 15-26, with figure 4b and at column 6, lines 41-67 and because of Pole, II et al's suggestion of integrating power management control logic into a host and a system bridge at column 4, lines 2-8. It would have been obvious for one of ordinary skill in the art to combine Pole, II

and Pole, II et al because they are both directed to the problem of placing a processor into a deep sleep state and transitioning the processor into a different operating/performance mode.

Per claims 7-10:

Pole, II describes a computer system comprising a memory (memory 216) and a memory controller with figure 2 and at column 4, lines 15-26. In addition, Pole, II et al describes a computer system comprising a memory (RAM 16), a memory controller (host bridge 18) and a power management controller (logic 100 and 102) with figures 1 and 2, at column 3, lines 15-24 and at column 4, lines 23-30. Pole, II et al describes performing a suspend to RAM transition with figure 4 and at column 7, line 51 – column 8, line 62. Pole, II et al describe that an ACPI driver (a BIOS component) indicates a suspend to RAM at column 7, lines 51-63. Pole, II describes placing only the processor in a reset sequence when changing processing modes with figure 4b and at column 6, lines 60-67.

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 703-305-9663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Dennis M. Butler

Dennis M. Butler
Primary Examiner
Art Unit 2115